AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior version, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A mating detection circuit constructed and arranged to determine whether at least one connector of an expansion card is mated with a corresponding connector of a computer system in which the expansion card is configured to be ~~installed.~~ installed, comprising:

at least one FET each configured to directly or indirectly monitor at least one signal presented at each of the at least one connector.

2. (Cancelled)

3. (Currently Amended) The circuit of ~~claim 2~~ claim 1, wherein for each of the at least one connector, each indirectly monitored signal is one of either ~~the same as,~~ provided by, derived from, related to, or controlled by the ~~associated~~ signal presented at the connector.

4. (Original) The circuit of claim 1, wherein the mating detection circuit generates at least one mating status signal each representing the mating status of a combination of one or more of the at least one connector.

5. (Original) The circuit of claim 4, wherein the at least one mating status signal is provided to the computer system.

6. (Original) The circuit of claim 5, wherein the at least one mating status signal controls a state of one or more bits in the computer system.

7. (Original) The circuit of claim 6, wherein the at least one mating status signal controls a state of a general purpose I/O (GPIO) bit.

8. (Currently Amended) The circuit of ~~claim 2~~ claim 1, wherein the at least one monitored signal comprises a voltage signal, ~~is voltage signals~~ and wherein the ~~mating detection circuit~~ at least one FET comprises:

~~at least one FET each having its source~~ a FET having a source coupled to a ground potential, ~~its gate~~ a gate driven by ~~an associated one of~~ the at least one monitored signal, and ~~its drain~~ a drain connected to a voltage source and an output node from which one of ~~the~~ at least one mating status signal is generated.

9. (Original) The circuit of claim 8, wherein the at least one FET comprises a plurality of FETs series connected to each other and wherein the at least one mating status signal comprises one mating status signal generated at the drain of one of the plurality of series-connected FETs located furthest from the ground potential.

10. (Original) The circuit of claim 1, wherein the mating detection circuit is located on the expansion card.

11. (Currently Amended) An expansion card for insertion into an expansion slot of a computer system, comprising:

at least one connector configured to mate with a corresponding connector of the computer system; and

a mating detector constructed and arranged to determine the mating status of a selected one or more of the at least one connector comprising at least one FET each configured to directly or indirectly monitor at least one signal presented at each of the at least one connector.

12. (Cancelled)

13. (Currently Amended) The expansion card of ~~claim 12~~ claim 11, wherein each indirectly monitored signal is one of either ~~the same as,~~ provided by, derived from, related to, or controlled by the ~~associated~~ signal presented at each of the at least one connector.

14. (Original) The expansion card of claim 11, wherein the mating detector generates at least one mating status signal each representing the mating status of a combination of one or more of the at least one connector.

15. (Original) The expansion card of claim 14, wherein the at least one mating status signal is provided to the computer system.

16. (Original) The expansion card of claim 15, wherein the at least one mating status signal controls a state of one or more bits in the computer system.

17. (Original) The expansion card of claim 16, wherein the at least one mating status signal controls a state of a general purpose I/O (GPIO) bit.

18. (Currently Amended) The expansion card of ~~claim 12~~ claim 11, wherein the at least one monitored signal is voltage signals and wherein the ~~mating detector~~ at least one FET comprises:

~~at least one FET each having its source~~ a FET having a source coupled to a ground potential, ~~its gate~~ a gate driven by ~~an associated one of~~ the at least one monitored signal, and ~~its drain~~ a drain connected to a voltage source and an output node from which one of ~~the~~ at least one mating status signal is generated.

19. (Original) The expansion card of claim 18, wherein the at least one FET comprises a plurality of FETs series connected to each other and wherein the at least one mating status signal comprises one mating status signal generated at the drain of one of the plurality of series-connected FETs located furthest from the ground potential.

20. (Currently Amended) The expansion card of claim 11, wherein the at least one connector ~~comprising~~ comprises one or more of the group consisting of:

at least one card connector and

at least one cable connector.

21. (Original) The expansion card of claim 20, wherein the at least one card connector comprises:

an Accelerated Graphics Port (AGP) card connector.

22. (Original) The expansion card of claim 20, wherein the at least one cable connector comprises one or more of the group consisting of:

a Universal Serial Bus (USB) cable connector; and

a power connector.

23. (Original) An expansion card for inserting into an expansion slot of a computer system, comprising:

at least one connector configured to mate with a corresponding connector of the computer system; and

means for determining whether a selected one or more of the at least one connector of the expansion card is mated with a corresponding connector of the computer system.

24. (Currently Amended) The expansion card of claim 23, wherein the determining means comprises:

means for directly or indirectly monitoring at least one signal each related to the mating status of the selected one or more connectors; and

means for generating at least one mating status signal each representing the mating status of any combination of one or more of the selected one or more connectors.

25. (Currently amended) The expansion card of claim 24, wherein each indirectly monitored signal is one of either ~~the same as,~~ provided by, derived from or controlled by the ~~associated~~ signal presented at each of the at least one connector.

26. (Original) The expansion card of claim 24, wherein the at least one mating status signal controls a state of one or more bits in the computer system.

27. (Currently Amended) A method for determining whether a connector of an expansion card is mated with a corresponding connector of a computer system having an expansion slot configured to receive the expansion card, comprising:

monitoring directly or indirectly at least one signal each related to the mating status of the selected one or more connectors, with at least one FET used for said monitoring; and

generating at least one mating status signal each representing the mating status of any combination of one or more of the selected one or more connectors.

28. (Currently Amended) The method of claim 27, wherein each indirectly monitored signal is one of either ~~the same as,~~ provided by, derived from, related to, or controlled by the ~~associated~~ signal presented at each of the at least one connector.